I claim:

1. An analog-to-digital converter, comprising:

a digitizer for producing a digital output signal from a sampled analog input signal;

a sample-and-hold circuit for storing a plurality of successive samples of said input signal; and

a control element for controlling switches to sequentially apply said stored samples to said digitizer in response to an activation signal so as to output a digitized version of said input signal as it existed prior to said activation signal.

2. An analog-to-digital converter as claimed in claim 1, wherein said sample-and-hold circuit comprises a plurality of sampling circuits connected to said digitizer through respective output switches controlled by said control element.

3. An analog-to-digital converter as claimed in claim 2, wherein said plurality of sampling circuits are each connected to said digitizer through respective input switches controlled by said control element.

4. An analog-to-digital converter as claimed in claim 3, wherein said sampling circuits each comprise a capacitor.

5. An analog-to-digital converter as claimed in claim 4, comprising eight said capacitors.

6. An analog-to-digital converter as claimed in claim 1, further comprising a comparator for generating said activation signal in response to said input signal reaching a threshold level.

7. An analog-to-digital converter as claimed in claim 1, wherein said control element is a state machine.

8. A method of converting an analog signal to a digital signal, comprising:

feeding said analog signal to a sample-and-hold circuit;

storing successive samples of said input signal in said sample-and-hold circuit; and

sequentially applying said stored samples with a delay of at least one sample

period to a digitizer in response to an activation signal, said digitizer producing a digital output signal representing said input signal as it existed prior to said activation signal.

9. A method as claimed in claim 8, wherein said samples are stored in a series of sampling circuits, each connected to said digitizer through respective output switches, and said samples are sequentially applied to said digitizer with a delay by controlling said output switches.

10. A method as claimed in claim 9, wherein said activation signal is generated by comparing said input signal with a predetermined threshold.

11. A method as claimed in claim 10, wherein said sampling circuits each comprise a capacitor.

12. A method as claimed in claim 11, wherein said sampling circuits comprise eight said capacitors.

13. A pacemaker comprising:

a front end for receiving an analog input signal including a comparator for comparing said input signal with a threshold value, said front end generating an activation signal when said input signal reaches said threshold value;

a sample-and-hold circuit for storing a plurality of successive samples of said input signal;

a digitizer; and

a control element for controlling switches to sequentially apply said stored samples to said digitizer in response to said activation signal so as to output a digitized version of said input signal as it existed prior to said activation signal.

14. A pacemaker as claimed in claim 13, wherein said sample-and-hold circuit comprises a plurality of sampling circuits connected to said digitizer through respective output switches controlled by said control element.

15. A pacemaker as claimed in claim 14, wherein said plurality of sampling circuits are each connected to said digitizer through respective input switches controlled by said control element.

16. A pacemaker as claimed in claim 13, further comprising a RAM for storing said digitized version of said input signal as it existed prior to said activation signal.

17. A pacemaker as claimed in claim 13, wherein said control element is a state machine.